

In The Claims:

Please cancel claims 1-11 without prejudice or disclaimer, and add claims 12-26 as follows:

12. (New) A semiconductor memory device comprising:

a memory transistor having a first terminal, a second terminal and a gate electrode;

a bitline;

a first select transistor connected between the first terminal of said memory transistor and said bitline; and

a programming circuit which applies a first voltage to a gate electrode of the first select transistor at a first time of programming, applies a second voltage to the gate electrode of the memory transistor at the first time of programming, applies a third voltage to the gate electrode of the first select transistor at a second time of programming after the first time, applies a programming voltage to the gate electrode of the memory transistor at the second time of programming, applies a program inhibition voltage to the bitline from the first time to the second time when the memory transistor is to be prevented from programming, and applies a plurality of program promotion voltages at the second time when the memory transistor is to be programmed,

wherein the first voltage is higher than the third and program inhibition voltages, the program promotion voltages are lower than the third and program inhibition voltages, and the second voltage is lower than the programming voltage.

13. (New) The device according to claim 12, wherein the second voltage has a same voltage as the third voltage.

14. (New) The device according to claim 12, wherein the third voltage has a same

voltage as the program inhibition voltage.

15. (New) The device according to claim 12, wherein the memory transistor stores data of more than one bit.

16. (New) The device according to claim 15, wherein the program promotion voltages are dependent on the data to be programmed.

17. (New) The device according to claim 12, further comprising a second select transistor connected to the second terminal of the memory transistor in order to control a current path of the memory transistor, wherein the second select transistor is non-conductive from the first time to the second time.

18. (New) A semiconductor memory device comprising:

a memory unit having a plurality of memory transistors connected in series and having a first end and a second end;

a first select transistor connected to the first end of said memory unit;

a second select transistor connected to the second end of said memory unit;

a bitline connected to the first end of said memory unit through the first select transistor;

and

a programming circuit which applies a first voltage to a gate electrode of the first select transistor at a first time of programming, applies a second voltage to a gate electrode of a selected memory transistor in the memory unit at the first time of programming, applies a third voltage to a gate electrode of a memory transistor other than the selected memory transistor in the memory unit at the first time of programming, applies a fourth voltage to the gate electrode of the first select transistor at a second time of programming after the first time, applies a

programming voltage to the gate electrode of the selected memory transistor at the second time of programming, applies a fifth voltage to the gate electrode of the memory transistor other than the selected memory transistor at the second time of programming, applies a program inhibition voltage to the bitline from the first time to the second time when the selected memory transistor is to be prevented from programming, and applies a plurality of program promotion voltages at the second time when the selected memory transistor is to be programmed,

wherein the first voltage is higher than the fourth and program inhibition voltages, the program promotion voltages are lower than the fourth and program inhibition voltages, the second voltage is lower than the programming voltage, and the third voltage is lower than the fifth voltage.

19. (New) The device according to claim 18, wherein the second voltage has a same voltage as the third voltage.

20. (New) The device according to claim 19, wherein the fourth voltage has the same voltage as the second and third voltages.

21. (New) The device according to claim 18, wherein the memory transistor other than the selected memory transistor is positioned between the selected memory transistor and the first select transistor.

22. (New) The device according to claim 21, wherein a memory transistor, which is adjacent to the selected memory transistor and is positioned between the selected memory transistor and the second select transistor, has a gate electrode connected to a ground voltage.

23. (New) The device according to claim 18, wherein the fourth voltage has a same voltage as the program inhibition voltage.

24. (New) The device according to claim 18, wherein each memory transistor stores data of more than one bit.

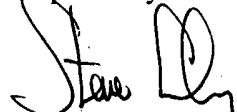
25. (New) The device according to claim 24, wherein the program promotion voltages are dependent on the data to be programmed.

26. (New) The device according to claim 18, wherein the second select transistor is non-conductive from the first time to the second time.

REMARKS

By this Amendment, claims 1-11 are canceled without prejudice or disclaimer, and claims 12-26 are added. Prompt and favorable examination on the merits is respectfully requested.

Respectfully submitted,

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